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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/899,573	ERRATICO, PIETRO
	Examiner	Art Unit
	Johannes P Mondt	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-31* is/are pending in the application.

4a) Of the above claim(s) *27-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4) ☐ Interview Summary (PTO-413) Paper No(s) _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

After-Final Response has been entered as Paper No. 14. In light of said response, the Final Rejection of Paper No. 13 is withdrawn and a new Final Rejection is herewith submitted.

The examiner agrees that Figure 14 in Chang et al does not represent a final structure and as such should not have been used in the Final Rejection of Paper No. 14. However, new rejections based on other prior art preclude allowance, as will be clarified below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. ***Claims 12-13 and 15-21*** are rejected under 35 U.S.C. 102(e) as being anticipated by Boden, Jr. (6,452,230 B1).

With regard to claim 12: With reference to Figures 1 and 3, Boden, Jr. teaches an integrated structure, comprising:

a substrate 11 (cf. column 2, lines 1-3) having a first conductivity type (N-type);

an epitaxial layer 12 (cf. column 2, lines 1-5) on said substrate and having the first conductivity type and a conductivity less than a conductivity of said substrate (N- as opposed to N+ for the substrate);

first and second regions (left – and right- portions of regions) 15 through 18 (and designated 70 in Figure 3) (cf. column 2, lines 10-19 and column 3, lines 8-21) in said epitaxial layer each having a second conductivity type opposite the first conductivity type (namely: P-type), said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and second junctions therewith (cf column 2, lines 10-25); and

an isolating element (e.g., 49, 50, 51, 75, 76) (cf. column 2, lines 31-44 and column 3, lines 13-16) positioned between said first and second regions (i.e., between the left and right portions of said regions 15, 16, 17, or 18; cf. Figure 1; or between the left and right portions of said region 70; cf. Figure 3) and extending from the surface of said epitaxial layer at least as far as a top surface of said substrate (inherently thus, hence "for") for reducing an injection of current through said epitaxial layer from said first region to said second region when the first junction is directly biased, said isolating

element comprising a dielectric material (silicon dioxide liner of trench 75; cf. Figure 3 and column 3, lines 13-21) adjacent said epitaxial layer and polycrystalline silicon 77 (column 3, lines 16) (cf. Figure 3) spaced apart from said epitaxial layer by said dielectric material (cf. column 3, lines 13-15), said isolating element also terminating above a bottom surface of said substrate (cf. Figure 3).

In conclusion, Boden, Jr. anticipates claim 12.

With regard to claim 13: said isolating element 75 at least partially surrounds said first region 70 (cf. Figure 3).

With regard to claims 15 and 20: Boden, Jr. teaches his invention for any particular first and second type conductivities (see claim 1 in Boden, Jr., column 3, line 29 – column 4, line 21).

With regard to claims 16 and 21: the first region as taught by Boden, Jr. comprises a power transistor (cf. column 1, lines 16-30 and 53-57), while it is inherent to power transistors that they are able to control an impedance including inductive load, as described in standard text books such as B. Jayant Baliga, "Modern Power Devices", Krieger Publishing Co., Malabar, Florida, reprint edition 1992, page 377.

With regard to claim 17: Boden, Jr. teaches (cf. Figs. 1 and 3) an integrated structure, comprising:

a substrate 11 having a first conductivity (n-type);

an epitaxial layer 12 on said first substrate and having first conductivity type and a conductivity less than that of the substrate;

first and second regions (left- and right-side portions of 15, 16, 17, 18, or 70; see column 2, lines 10-25) in said epitaxial layer each having second conductivity type opposite the first conductivity type (namely: p-type), said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and second junctions therewith; and

an isolating element (e.g., 49, 50, 51, 75, 76) (cf. column 2, lines 31-44 and column 3, lines 13-16) positioned between said first and second regions (i.e., between the left and right portions of said regions 15, 16, 17, or 18; cf. Figure 1; or between the left and right portions of said region 70; cf. Figure 3) and extending from the surface of said epitaxial layer at least as far as a top surface of said substrate (cf. Figures 1 and 3; cf. column 2, lines 27-37), said isolating element partially surrounding at least one of said first and second regions, said isolating element also terminating above a bottom surface of said substrate (cf. Figs. 1 and 3).

With regard to claim 18: said isolating element comprises a dielectric material (cf. column 3. lines 13-16).

With regard to claim 19: said isolating element further comprises polycrystalline silicon (cf. column 3, lines 13-16).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claim 14 and 22-26*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Boden, Jr. in view of Nakagawa (6,239465 B1).

With regard to claim 14: As detailed above, Boden, Jr. anticipates claim 12. Boden, Jr. does not necessarily teach the further limitation as defined by claim 14. However, Nakagawa teaches isolation trenches for prevention of electrical interference between different portions of the device and with a length substantially equal to the width of the chip (cf. Figures 5 and 8).

Motivation to include the teaching by Nakagawa in the invention of Boden, Jr., is the purpose for which the trench is made, namely: to prevent a current path between the different portion of the device: that is what (electrical) isolation element means. Combination of the inventions is easily accomplished as no other limitation pertains to the direction along the width of the chip while any part of the chip in Boden, Jr. not provided with the trench isolation is clearly not substantial to the invention, said trench isolation being shown on each and every embodiment. For the above reasons it would have been obvious to improve the invention by Boden, Jr. in accordance with the abovementioned teaching by Nakagawa so as to accentuate the role and function of the isolation element as taught by Boden, Jr.

With regard to claim 22: With reference to Figures 1 and 3, Boden, Jr. teaches an integrated structure, comprising:

a substrate 11 (cf. column 2, lines 1-3) having a first conductivity type (N-type);

an epitaxial layer 12 (cf. column 2, lines 1-5) on said substrate and having the first conductivity type and a conductivity less than a conductivity of said substrate (N- as opposed to N+ for the substrate);

first and second regions (left – and right- portions of regions) 15 through 18 (and designated 70 in Figure 3) (cf. column 2, lines 10-19 and column 3, lines 8-21) in said epitaxial layer each having a second conductivity type opposite the first conductivity type (namely: P-type), said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and second junctions therewith (cf. column 2, lines 10-25); and

an isolating element (e.g., 49, 50, 51, 75, 76) (cf. column 2, lines 31-44 and column 3, lines 13-16) positioned between said first and second regions (i.e., between the left and right portions of said regions 15, 16, 17, or 18; cf. Figure 1; or between the left and right portions of said region 70; cf. Figure 3) and extending from the surface of said epitaxial layer at least as far as a top surface of said substrate, said isolating element terminating above a bottom surface of said substrate.

Boden, Jr. does not necessarily teach the further limitation that said isolating element should have "a length substantially equal to a width of the semiconductor chip and dividing the semiconductor chip into two portions each respectively including said first and second regions". However, Nakagawa teaches isolation trenches for prevention of electrical interference between different superficial portions of the device and with a length substantially equal to the width of the chip (cf. Figures 5 and 8) and such that

each of said portions include said first and second regions (numeral 28 in Nakagawa; see also Figure 3 in Nakagawa).

Motivation to include the teaching by Nakagawa in the invention of Boden, Jr., is the purpose for which the trench is made, namely: to prevent a current path between the different portion of the device: that is what (electrical) isolation element means. Combination of the inventions is easily accomplished as no other limitation pertains to the direction along the width of the chip while any part of the chip in Boden, Jr. not provided with the trench isolation is clearly not substantial to the invention, said trench isolation being shown on each and every embodiment. For the above reasons it would have been obvious to improve the invention by Boden, Jr. in accordance with the abovementioned teaching by Nakagawa so as to accentuate the role and function of the isolation element as taught by Boden, Jr.

With regard to claims 23-24: said isolating element as taught by Boden Jr. comprises a dielectric and further comprised polycrystalline silicon (cf. column 3, lines 13-16).

With regard to claim 25: Boden, Jr. teaches his invention for any particular first and second type conductivities (see claim 1 in Boden, Jr., column 3, line 29 – column 4, line 21).

With regard to claim 26: the first region as taught by Boden, Jr. comprises a power transistor (cf. column 1, lines 16-30 and 53-57), while it is inherent to power transistors that they are able to control an impedance including inductive load, as

described in standard text books such as B. Jayant Baliga, "Modern Power Devices", Krieger Publishing Co., Malabar, Florida, reprint edition 1992, page 377.

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Blanchard (5,034,785).

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action. Any inquiry concerning this communication or earlier communications from the examiner should be directed to

Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
February 13, 2003